**Amendments to the Claims**

This listing of claims will replace all prior versions and listings of claims in the application.

**Listing of Claims**

1. (Currently Amended) A method for fabricating a shallow trench isolation region, comprising:

forming an intermediate layer upon an upper surface of a semiconductor topography, wherein the intermediate layer comprises a doped oxide layer;

forming one or more trenches within the intermediate layer and the semiconductor topography;

blanket depositing a trench fill material over ~~a semiconductor topography comprising~~and within the one or more trenches;

polishing the ~~semiconductor topography~~trench fill material with an abrasive polishing surface in the absence of a fluid or in the presence of a fluid that is substantially free of particulate matter to form an upper surface ~~of the semiconductor topography~~ at an elevation above the trenches, wherein the upper surface does not comprise a polish stop material; and

etching an entirety of the upper surface simultaneously, wherein remaining portions of the trench fill material are laterally confined within the trenches.

2. (Original) The method of claim 1, wherein an upper surface of the remaining portions is above an upper surface of a semiconductor substrate within the semiconductor topography.

3. (Original) The method of claim 2, wherein said upper surface of the remaining portions is less than approximately 200 angstroms above the upper surface of the semiconductor substrate.

4. (Currently Amended) The method of claim 1, wherein the step of polishing comprises inserting ~~the~~ a fluid consisting essentially of water between the ~~semiconductor topography~~trench fill material and the abrasive polishing surface.

5. (Currently Amended) he method of claim 1, ~~further comprising forming an intermediate layer upon an upper surface of the semiconductor topography prior to said depositing trench fill material, and~~ wherein said etching comprises etching at least a portion of the ~~intermediate~~ doped oxide layer.

6. (Currently Amended) The method of claim ~~5~~1, wherein said intermediate layer further comprises a base oxide layer.

7. (Canceled)

8. (Currently Amended) The method of claim ~~7~~1, wherein said doped oxide layer comprises borophosphosilicate glass.

9. (Currently Amended) The method of claim ~~5~~1, wherein said intermediate layer further comprises a nitride layer, and wherein a thickness of said nitride layer is less than approximately 500 angstroms.

10. – 11. (Canceled)

12. (Currently Amended) A method for processing a semiconductor topography, comprising:

polishing an upper layer of said semiconductor topography with an abrasive polishing surface in the ~~absence of a fluid or in the~~ presence of a fluid that is substantially free of particulate matter to form an upper surface of the semiconductor topography at an elevation above an underlying layer, wherein the underlying layer comprises a lateral variation in polishing characteristics, and wherein the step of polishing comprises inserting a fluid consisting essentially of water between the semiconductor topography and the abrasive polishing surface; and

etching the entirety of the upper surface of the semiconductor topography simultaneously to expose the underlying layer.

13. (Original) The method of claim 12, wherein said upper surface of the semiconductor topography is spaced sufficiently above the underlying layer to avoid dishing during said polishing.

14. (Original) The method of claim 12, wherein said upper surface of the semiconductor topography is spaced sufficiently above the underlying layer to avoid polishing the underlying layer.

15. (Original) The method of claim 12, wherein said elevation is between approximately 100 angstroms and approximately 1000 angstroms.

16. (Canceled)

17. (Original) The method of claim 12, wherein said upper layer comprises an interlevel dielectric layer.

18. (Original) The method of claim 17, wherein said interlevel dielectric layer comprises silicon dioxide.

19. (Original) The method of claim 12, wherein said underlying layer comprises a silicon substrate patterned with dielectric filled trenches.

20. – 21. (Canceled)

22. (Previously Presented) A method for processing a semiconductor topography, comprising polishing a dielectric layer with an abrasive polishing surface in the absence of a fluid or in the presence of a fluid consisting essentially of water for reducing a required thickness of an additional layer underlying the dielectric layer.

23. (Original) The method of claim 22, wherein said additional layer has different polishing characteristics than the dielectric layer.

24. (Original) The method of claim 22, wherein said reducing comprises forming the additional layer with a thickness of less than approximately 500 angstroms.

25. (Original) The method of claim 22, wherein said reducing comprises forming the additional layer with a thickness of approximately 150 angstroms or less.

26. (Original) The method of claim 22, wherein said reducing comprises eliminating the additional layer.

27. (Original) The method of claim 22, wherein the dielectric layer comprises a trench fill layer for shallow trench isolation regions.

28. (Original) The method of claim 22, wherein the dielectric layer comprises an interlevel dielectric layer.

29. (Previously Presented) The method of claim 22, wherein the step of polishing comprises applying a fluid substantially free of particulate matter between the semiconductor topography and an abrasive polishing surface.

30. (Previously Presented) The method of claim 22, further comprising etching the dielectric layer subsequent to the step of polishing the dielectric layer.

31. (New) The method of claim 12, further comprising:

forming an intermediate layer upon an upper surface of the semiconductor topography;

forming one or more trenches within the intermediate layer and the semiconductor topography; and

blanket depositing the upper layer over and within the one or more trenches prior to the step of polishing the upper layer.

32. (New) The method of claim 31, wherein the intermediate layer comprises a doped oxide layer.

33. (New) The method of claim 32, wherein said doped oxide layer comprises borophosphosilicate glass.

34. (New) The method of claim 31, wherein said intermediate layer comprises a nitride layer with a thickness of less than approximately 500 angstroms.

35. (New) The method of claim 31, wherein said intermediate layer further comprises a silicon carbide layer.

36. (New) The method of claim 31, wherein said intermediate layer further comprises a carbonated polymer layer.